UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/749,725	12/28/2000	James S. Burns	042390.P10120	6772

45209 7590 03/17/2008

INTEL/BLAKELY
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
03/17/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/749,725	BURNS ET AL.	
	Examiner	Art Unit	
	AIMEE J. LI	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-8,10-15,17 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-8,10-15,17 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 2, 4-8, 10-15, 17, and 18 have been examined. Claims 1, 7, and 13 have been amended as per Applicants' request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE as filed 04 January 2008; Amendment as filed 04 January 2008; and Power of Attorney as filed 17 January 2008.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04 January 2008 has been entered.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, 4-8, 10-15, 17, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Hirata et al., U.S. Patent Number 5,430,851.

6. In regard to claim 1, Hirata et al. disclose a processor (col. 4, line 50), comprising:

a. A plurality of pipelined functional units for executing instructions (Fig. 3, elements 16-18);

b. A centralized scheduler (Fig. 4, instruction setup units 34 and instruction schedule unit 35 [col. 9, lines 36-45]), coupled to the plurality of functional units (fig. 4, 16-18),

c. Wherein the centralized scheduler is programmed to receive via an instruction buffer and an instruction decoder at least two separate instruction groups (column 4, line 50 to column 5, line 4), in a first stage (fig. 4, instruction setup units 34 comprise of the first stage) map each of the at least two separate instruction groups to at least a portion of the functional units independently of each other in which the centralized scheduler treats each instruction group as having full access and availability to the plurality of pipelined functional units (independent instruction setup units for each instruction stream [col. 5, lines 55-59] map instructions to functional units by setting a type tag T [col. 6, lines 19-20, 25-27]), and based at least in part on functional unit availability and instruction dependencies (signal R, col. 6, lines 54-56), perform a merging (col. 6, lines 11-14, instruction schedule unit merges the instructions from each of the instruction groups) and remapping of the at least two separate instruction groups to the at least a portion of the functional units (col. 8, lines 48-56, instruction schedule unit remaps the instructions based on resource conflicts) in a second stage to ensure that no resource conflict occurs between the plurality of pipelined functional units (fig. 4, instruction schedule unit 35 comprises of a second stage)

7. In regard to claim 2, Hirata et al. further disclose that the scheduler is programmed to deliver the instruction to the portion of functional units following merging and remapping (instructions are sent to the functional units from the instruction schedule unit 35 which is responsible for the merging and remapping, fig. 4 and col. 8, 51-56).

8. In regard to claim 4, Hirata et al. further disclose that at least a portion of the functional units execute instructions from the at least two instruction groups (col. 5, 40-44; col. 6, 25-34).

9. In regard to claim 5, Hirata et al. further disclose that the instruction groups (instruction streams) follow a simultaneous multi-threading structure (col. 2, lines 65-68).

10. In regard to claim 6, Hirata et al. further disclose that the instruction groups are prioritized to prevent pipeline failures (resulting from contention) during execution of instructions (col. 7, 65-68; col. 8, 1-10).

11. In regard to claims 7 and 13, Hirata et al. disclose a method of dispersing instructions (instruction schedule unit distributes instructions to the functional units, col. 6, lines11-14) to be executed by a processor (col. 4, line 50), comprising:

a. Receive at least two separate instruction groups in a scheduler via an instruction buffer and an instruction decoder (column 4, line 50 to column 5, line 4);

b. In a first stage of the scheduler (instruction setup unit 34), map (instruction setup units [fig. 4, 34] map instructions to functional units by setting a type tag T [col. 6, lines 19-20, 25-27]) each of the at least two separate instruction groups (instruction streams, col. 5, lines 55-59) to at least a portion of functional units independently of each other (instruction setup unit 34); and

c. Based at least in part on functional unit availability and instruction dependencies (signal R, col. 6, lines 54-56), perform a merging (col. 6, lines 11-14, instruction schedule unit merges the instructions from each of the instruction groups) and remapping (col. 8, lines 48-56, instruction schedule unit remaps the instructions based on resource conflicts) of the at least two separate instruction groups to the at least a portion of functional units (col. 9, lines 46-64: the instruction schedule unit 35 receives an instruction subgroup of up to 2 instructions from the instruction stream being fetched) in a second stage of the scheduler (instruction schedule unit 15).

12. In regard to claims 8 and 14, Hirata et al. further disclose the step of delivering the instructions to portions of functional units following merging and remapping (instructions are sent to the functional units from the instruction schedule unit which is responsible for the merging and remapping, fig. 4 and col. 8, 51-56).

13. In regard to claims 10 and 15, Hirata et al. further disclose at least a portion of the functional units execute instructions from the at least two instruction groups (col. 5, 40-44; col. 6, 25-34).

14. In regard to claims 11 and 17, Hirata et al. further disclose that the instruction groups (instruction streams) follow a simultaneous multi-threading structure (col. 2, lines 65-68).

15. In regard to claims 12 and 18, Hirata et al. further disclose that the instruction groups are prioritized to prevent pipeline failures (resulting from contention) during execution of instructions (col. 7, 65-68; col. 8, 1-10).

Response to Arguments

16. Applicant's arguments filed 04 January 2008 have been fully considered but they are not persuasive.

17. Applicant argues in essence on page 5

> …The cited art, including Hirata, fails to teach or suggest this subject matter. In this regard, scheduler unit 15 of Hirata does not perform these two stages of operation….Furthermore, there is not two separate mappings, namely a mapping and then a later merging and remapping of these groups…

18. This has not been found persuasive. As shown in the rejection above, these limitations were taught by Hirata. Hirata discloses in column 4, line 50 to column 5, line 4 that instructions of multiple independent instruction streams, i.e. instruction groups, are fetched from an instruction cache and sent through a decoder. Even though the initial scheduling stage of determining whether the functional units are needed are not is part of the operation of the decode unit, there are other operations to decoding the instruction, such as determining the exact operation to be performed and its associated operands and control signals. Hirata teaches in the cited segments above that the instructions have full access to all the pipelined functional units and that resource conflict is managed in the second part of the scheduling where the merging and remapping takes place based upon the resource conflict management. The Examiner would also note that the full access to pipelined execution units and ensuring no resource conflict limitations in claim 1 are not explicitly recited in the other two independent claims 7 and 13.

19. Applicant argues in essence on page 5

> …Furthermore, there is not two separate mappings, namely a mapping and then a later merging and remapping of these groups...

20. This has not been found persuasive. As the Examiner explained in the previous responses, Hirata describes in column 6, lines 3-7 that the decode unit decides the instructions and outputs the instruction to the schedule unit "if it [the instruction] should be executed in the function execution units". This means that the decode units need to make a preliminary determination if the execution units are needed, e.g. a mapping to the entire set of functional units. Simply moving this initial mapping from taking place in the decode unit to the scheduler, as is suggested by the arguments, is not a patentable matter (Please see *In re Japikse*, 181 F.2d 1019, 86 USPQ 70 (CCPA 1950)). Hirata then describes in column 6, lines 11-14 and 19-34 the scheduler performs another mapping, e.g. remapping, of the instructions to a specific functional unit within the group of functional units. Hirata describes in column 14, line 49 to column 15, line 3 and column 16, line 57 to column 17, line 10 having instructions held in a stand-by area by the scheduler based upon dependencies and in column 44, lines 11-19 that instructions are only issued to a functional unit by the scheduler when the functional unit is available. Hirata also describes in column 5, lines 5-9 and 61-64 and column 6, lines 11-14 that the scheduler merges the instructions streams, so they are all executed together in the functional units. Therefore, Hirata performs a mapping of the instruction groups in the decide unit and then the scheduler merges and remaps the instructions based upon functional unit availability and resource dependencies.

21. Also, Hirata discloses in column 9, lines 8-33 that there are other embodiments in which the functional units are homogeneous and shows this in Figure 9 with two functional units 16.

The system then first maps an instruction with the decoder to the functional units and the scheduler chooses the functional unit based on resource dependencies and availability of the functional unit. In the case of an integer instruction that is to be executed in functional unit 16, the decoder would determine that a functional unit is needed, i.e. the first stage mapping, and the scheduler would send the instruction to the next available integer functional unit 16 after the resource dependencies are resolved, i.e. the second stage remapping/merging. The decoding of an instruction and the scheduling of the instruction are two separate stages in the pipeline.

22. In addition, there is nothing in the claim language that specifically recites the decoder and scheduler are two separate entities that do not have cross over functionality.

Conclusion

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to AIMEE J. LI whose telephone number is (571)272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

24. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

25. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated

information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aimee J Li/
Primary Examiner, Art Unit 2183
2 March 2008